IN THE CLAIMS

Listing of Claims

1. – 14. (Canceled)

15.   (Previously Presented) A method for writing clear data to a frame buffer of a graphics display device, comprising:

determining a dimension and a position of at least one image displayed on said graphics display device, wherein said at least one image is to be cleared;

determining a location of a region of memory where a plurality of data having at least pixel information associated with a plurality of pixels which display said at least one image is stored;

subdividing said memory region into a plurality of sub-regions; and

writing said clear data concurrently to each of said plurality of sub-regions.

16.   (Previously Presented) The method of claim 15, further comprising issuing one clear command which initiates said writing said clear data concurrently.

17.   (Previously Presented) The method of claim 15, further comprising issuing a plurality of clear commands, wherein each one of said clear commands corresponds to one of each said plurality of sub-regions, and wherein the issuing said plurality of clear commands initiates said writing said clear data concurrently.

18.   (Previously Presented) The method of claim 15, further comprising associating a plurality of location identifiers, wherein one location identifier is associated

with each one of said plurality of sub-regions residing in said frame buffer, and wherein said concurrently writing clear data begins at said plurality of sub-regions identified by said plurality of corresponding location identifiers.

19.   (Previously Presented) The method of claim 15, further comprising determining said dimension and said position for each one of a plurality of images, and repeating the determining a location and the subdividing for each one of said plurality of images.

20.   (Previously Presented) A computer-readable medium having a program for clearing data residing in a memory region, the program comprising logic configured to:

determine a dimension and a position of at least one image displayed on a video display device, wherein said at least one image is to be cleared;

determine a location of said memory region where a plurality of data having at least pixel information associated with a plurality of pixels which display said at least one image is stored;

subdivide said memory region into a plurality of sub-regions; and

write said clear data concurrently to each of said plurality of sub-regions.

21.   (Original) A system for clearing data residing in a memory region, comprising:

means for determining a dimension and a position of at least one image displayed on said graphics display device, wherein said at least one image is to be cleared;

means for determining a location of a region of memory where a plurality of data having at least pixel information associated with a plurality of pixels which display said at least one image is stored;

means for subdividing said memory region into a plurality of sub-regions; and

means for writing said clear data concurrently to each of said plurality of sub-regions.

22.   (Original) The system of claim 21, further comprising means for associating a plurality of location identifiers, wherein one location identifier is associated with each one of said plurality of sub-regions residing in said frame buffer, and wherein said means for concurrently writing clear data begins at said plurality of sub-regions identified by said plurality of corresponding location identifiers.

23.   (Original) The system of claim 22, further comprising means for determining said dimension and said position for each one of a plurality of images, and wherein said means of determining a location and said means for subdividing said memory region operates on each one of said plurality of images.

24.   (Previously Presented) A graphics system comprising:

a frame buffer; and

a pseudo-linear frame buffer control logic for clearing data in the frame buffer, the

pseudo-linear frame buffer control logic configured to:

        determine a region of the frame buffer to be cleared;

        subdivide the region of the frame buffer into a plurality of sub-regions; and

        concurrently write clear data to each of the plurality of sub-regions.

25.   (Previously Presented) The graphics system of claim 24, wherein the pseudo-

linear frame buffer control logic is configured to subdivide the region of the frame buffer to

be cleared into consecutive and adjacent sub-regions.

26.   (Previously Presented) The graphics system of claim 24, wherein the pseudo-

linear frame buffer control logic is configured to subdivide the region of the frame buffer to

be cleared into sub-regions that vary in dimension.

27.   (Previously Presented) The graphics system of claim 24, wherein the clear data

written to each of the plurality of sub-regions corresponds to a predefined color of a pixel.

28.   (Previously Presented) The graphics system of claim 24, wherein the pseudo-

linear frame buffer control logic is further configured to:

        determine a dimension and a position of at least one image displayed on a video

display device which is to be cleared; and

        determine a location of the at least one image in the region of the frame buffer.